S/N TBD

Docket: CS03-050

Group art unit: TBD

Date 01/21/2004

To: Commissioner of Patents and Trademarks

P.O. Box 1450 Alexandria, VA 22313-1450

Fr: William J. Stoffel Reg. No. 39,390 CUST NO. 30402

PMB 455

1735 Market St - Suite A Philadelphia, PA 19103

Subject:

Serial No. TDB

Docket cs03-050

File Date: with application

Inventor: Chui et al.

title: STRUCTURE AND METHOD TO FORM SOURCE AND DRAIN

REGIONS OVER DEPLETION DOPED REGIONS

Group art unit: TBD

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO A820 (also PTO-1449), Information Disclosure Citation and references.

CERTIFICATE OF MAILING OR EXPRESS MAILING

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William J. Stoffel Reg. No. 39,390

Customer number 30402

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The following Patents and/or Publication are submitted to comply with the duty to disclose under CFR 1.97-1.99 and 37 CFR 1.56.

US 6,383,883B1 (Chen et al.) shows a graded S/D region.

US 6,348,372B1 (Burr) shows a Method to reduce S/D junction capacitance.

US 2003/0132452 A1(Boriuchi) shows a recombination region.

US 5,795,803 (Takamura et al.) shows a well process.

US 6,528,826B2(Yoshida et al.) shows a device.

US 2002-009364A1(Inaba) shows a semiconductor device.

US 5,712,204 (Horiuchi) shows a method for S/D regions.

Inaba, et al., "Silicon on Depletion layer FET (SODEL FET) for sub-50 nm high performance CMOS applications: novel channel and S/D profile engineering schemes by selective Si epitaxial growth technology"., 2002, IEEE.

Sincerely,

William J. Stoffel

Reg. No. 39,390

Customer number 30,402

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			U. S. PATENT	DOCUMENTS	Pages, Columns, Lines, Where
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ^{2 (f known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Relevant Passages or Relevant Figures Appear
	-	US- 6, 3 83, 853 B1		Chanct al,	
	<u> </u>	US- 6, 348, 372 B1		Burr	
		US-2003/0152 452	}	Borruch; Takamura	
	Ī	US- 5775, 803		Takamura	
		US- /.			
		US- 6,528, 326.B2		Yushida	-
	<u> </u>	US-		1-4	
,	ļ	US- 2002/009364 A1		traba	
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Examiner Initials*	Cite No.1	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
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		NON PATENT LITERATURE DOCUMENTS	
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		Inaba, et al., "silicon on depletion layer FET (SODEL FET) for sub - 50 nm high performance by selective Si epi growth technology, 2002, IEEE	

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